WHAT IS CLAIMED IS:

1. A non-volatile memory cell comprising:

a substrate of a substantially single crystalline semiconductive material having a first conductivity type;

a first region of a second conductivity type in said substrate;

a second region of said second conductivity type in said substrate, spaced apart from said first region;

a channel region between said first region and said second region, said channel region having a first portion and a second portion;

a control gate insulated from said second portion of said channel region;

a floating gate adjacent to said control gate and insulated therefrom, and insulated from said first portion of said channel region, said floating gate having a tip adjacent to said control gate;

an erase gate insulated from said control gate and said tip of said floating gate; and

an insulating material between said tip and said erase gate permitting charges to tunnel from said tip to said erase gate.

2. The cell of claim 1 wherein said substrate is single crystalline silicon.

3. The cell of claim 2 wherein said substrate has a substantially planar surface and wherein said first region, said second region, and said channel region are along said planar surface.

4. The cell of claim 3 wherein said insulating material is silicon dioxide.

5. The cell of claim 4 wherein said floating gate is insulated from said planar surface by a layer of silicon dioxide.

6. The cell of claim 5 wherein said floating gate is insulated from said control gate by a layer of silicon nitride.

7. The cell of claim 6 wherein said control gate is insulated from said planar surface by a layer of silicon dioxide.

8. The cell of claim 7 wherein said floating gate is capacitively coupled to said first region.

9. The cell of claim 2 wherein said substrate has a substantially planar surface with a first trench and a second trench in said surface, with each trench having a bottom and a sidewall; and wherein said channel region having three portions: a first portion along a sidewall of said first trench, a second portion along said planar surface, and a third portion along a sidewall of said second trench; wherein said floating gate insulated from said first portion of said channel region gate and is in said first trench; wherein said cell further comprising:

a second floating gate adjacent to said control gate and insulated therefrom, and in said second trench and insulated from said third portion of said channel region, said second floating gate having a tip adjacent to said control gate; and

wherein said erase gate is insulated from said control gate and said tip of said first floating gate and said tip of said second floating gate;

an insulating material between said tip of said second floating gate and said erase gate permitting charges to tunnel from said tip of said second floating gate to said erase gate; and

wherein said first region is along said bottom of said first trench and said second region is along said bottom of said second trench.

10. The cell of claim 9 wherein said insulating material is silicon dioxide.

11. The cell of claim 10 wherein each of said first and second floating gates is insulated from said substrate by a layer of silicon dioxide.

12. The cell of claim 11 wherein each of said first and second floating gates is insulated from said control gate by a layer of silicon nitride.

13. The cell of claim 12 wherein said control gate is insulated from said planar surface by a layer of silicon dioxide.

14. An array of non-volatile memory cells comprising:

a substrate of a substantially single crystalline semiconductive material having a first conductivity type;

a plurality of non-volatile memory cells arranged in a plurality of columns and rows in said substrate, each of said non-volatile memory cells comprising:

a first region of a second conductivity type in said substrate;

a second region of said second conductivity type in said substrate, spaced apart from said first region;

a channel region between said first region and said second region, said channel region having a first portion and a second portion;

a control gate insulated from said second portion of said channel region;

a floating gate adjacent to said control gate and insulated therefrom, and insulated from said first portion of said channel region, said floating gate having a tip adjacent to said control gate;

an erase gate insulated from said control gate and said tip of said floating gate; and

an insulating material between said tip and said erase gate permitting charges to tunnel from said tip to said erase gate;

wherein the cells in the same row have their first regions connected together.

15. The array of claim 14 wherein said substrate is single crystalline silicon.

16. The array of claim 15 wherein the cells in the same row have their control gates connected together and have their erase gates connected together, and wherein cells in the same column have their second regions connected together.

17. The array of claim 16 wherein said substrate has a substantially planar surface and wherein said first region, said second region, and said channel region are along said planar surface.

18. The array of claim 17 wherein said insulating material is silicon dioxide.

19. The array of claim 18 wherein said floating gate is insulated from said substrate by a layer of silicon dioxide.

20. The array of claim 19 wherein said floating gate is insulated from said control gate by a layer of silicon nitride.

21. The array of claim 20 wherein said control gate is insulated from said planar surface by a layer of silicon dioxide.

22. The array of claim 21 wherein said floating gate is capacitively coupled to said first region.

23. The array of claim 15 wherein the cells in the same row have their second regions connected together, and wherein cells in the same column have their control gates connected together and have their erase gates connected together.

24. The array of claim 23 wherein said substrate has a substantially planar surface with a first trench and a second trench in said surface with each trench having a bottom and a sidewall; and wherein said channel region having three portions: a first portion along a sidewall of said first trench, a second portion along said planar surface, and a third portion along a sidewall of said second trench; wherein said floating gate is insulated from said first portion of said channel region and is in said first trench; wherein said cell further comprising:

a second floating gate adjacent to said control gate and insulated therefrom, and in said second trench and insulated from said third portion of said channel region, said second floating gate having a tip adjacent to said control gate; and

wherein said erase gate is insulated from said control gate and said tip of said first floating gate and said tip of said second floating gate;

an insulating material between said tip of said second floating gate and said erase gate permitting charges to tunnel from said tip of said second floating gate to said erase gate; and

wherein said first region is along said bottom of said first trench and said second region is along said bottom of said second trench.

25. The array of claim 24 wherein said insulating material is silicon dioxide.

26. The array of claim 25 wherein each of said first and second floating gates is insulated from said planar surface by a layer of silicon dioxide.

27. The array of claim 26 wherein each of said first and second floating gates is insulated from said control gate by a layer of silicon nitride.

28. The array of claim 27 wherein said control gate is insulated from said planar surface by a layer of silicon dioxide.

29. A method of making an array of non-volatile memory cells in a semiconductor substrate of a first conductivity having a planar surface, with a plurality of spaced apart floating gates insulated from said substrate with each floating gate capacitively coupled to a first region of a second conductivity in said substrate, said method comprising:

forming a plurality of word lines on said surface and insulated therefrom, each word line being between a pair of floating gates and adjacent and insulated from said floating gates;

forming a tunnel oxide layer on said word line and said floating gates; and

forming an erase gate on said tunnel oxide layer.

30. The method of claim 29 wherein each floating gate has a tip adjacent to said word line.

31. The method of claim 30 wherein said tunnel oxide layer is between said tip and said erase gate.

32. The method of claim 31 further comprising:

etching said erase gate and said word line in a region between said floating gates to form an erase gate and a word line associated with each floating gate and adjacent thereto; and

forming a second region of a second conductivity in said substrate between a pair of word lines.

33. The method of claim 32 further comprising:

wherein said word line connects cells in the same row in a first direction;

said erase gate connects cells in the same row in said first direction;

said first region connects cells in the same row in said first direction; and

said second region connects cells in the same column in a second direction substantially perpendicular to said first direction.

34. The method of claim 31 further comprising:

etching said substrate to form a first trench and a second trench with each trench having a bottom and a side wall;

forming said first region along said bottom of said first trench;

forming a second region of said second conductivity type along said bottom of said second trench;

wherein said floating gate is formed in said first trench, spaced apart and insulated from said sidewall; and

forming a second floating gate in said second trench, spaced apart and insulated from said sidewall.

35. The method of claim 34 further comprising:

wherein said word line connects cells in the same row in a first direction;

wherein said first region connects cells in the same column in a second direction, substantially perpendicular to said first direction;

said second region connects cells in the same column in said second direction; and

wherein said erase gate connects a plurality of cells from a plurality of adjacent columns and a plurality of adjacent rows.